then, removing the metal layer (as well as the capping layer, if any) from those MOS transistor structures where metal salicide exclusion regions are to be formed;

IN THE CLAIMS:

Amend claims 1, 2, 3, 5, 8, 9, 10, and 12 to read as follows (the attached appendix sets forth the amended claims with markings showing the differences between the original text and the text as hereby amended):

1. (Amended) A method for forming metal salicide regions and metal salicide exclusion regions during the manufacturing of an integrated circuit (IC), the method comprising the steps of:

(a) providing an IC structure including a plurality of MOS transistor structures, the plurality of MOS transistor structures having exposed silicon surfaces;

(b) depositing a metal layer on the IC structure in a controlled manner;

(c) forming a photoresist masking layer on portions of the MOS transistor structures where metal salicide regions are to be formed;

(d) removing the metal layer from those MOS transistor structures where metal salicide exclusion regions are to be formed;

(e) after step (d), stripping the photoresist masking layer; and

(f) after step (e), reacting metal in the metal layer with silicon in the exposed silicon surfaces to form metal salicide regions, wherein

step (b) includes the step of controlling at least one metal deposition parameter such that the metal layer has at least one predetermined property, and the at least one predetermined property limits metal salicide crawl during step (f) beyond at least one of the portions of the MOS transistor structures where metal salicide regions are to be formed.

2. (Amended) The method of claim 1, wherein said at least one predetermined property is such that at least one of the metal salicide regions has a predetermined sheet resistance.

A3 cont'd

3. (Amended) The method of claim 1, wherein said at least one predetermined property is such that at least one of the metal salicide regions has a predetermined conductivity.

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5. (Amended) The method of claim 1, wherein the removal during step (d) of the metal layer from those MOS transistor structures where metal salicide exclusion regions are to be formed, and step (b), are performed in a manner significantly limiting metal salicide crawl during step (f) over and under at least one of the portions of the MOS structures where metal salicide regions are to be formed.

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A5

8. (Amended) A method for forming cobalt salicide regions and cobalt salicide exclusion regions during the manufacturing of an integrated circuit (IC), the method comprising the steps of:

(a) providing an IC structure including a plurality of MOS transistor structures, the plurality of MOS transistor structures having exposed silicon surfaces;

(b) depositing a cobalt layer on the IC structure in a controlled manner;

(c) depositing a capping layer on the cobalt layer;

(d) forming a photoresist masking layer on portions of the MOS transistor structures where cobalt salicide regions are to be formed;

(e) removing the capping layer and the cobalt layer from those MOS transistor structures where cobalt salicide exclusion regions are to be formed;

(f) after step (e), stripping the photoresist masking layer; and

(g) after step (f), reacting cobalt in the cobalt layer with silicon in the exposed silicon surfaces to form cobalt salicide regions, wherein

step (b) includes the step of controlling at least one metal deposition parameter such that the cobalt layer has at least one predetermined property, and the at least one predetermined property limits cobalt salicide crawl during step (g) beyond at least one of the portions of the MOS transistor structures where cobalt salicide regions are to be formed.

9. (Amended) The method of claim 8, wherein said at least one predetermined property is such that at least one of the cobalt salicide regions has a predetermined sheet resistance.

A5 cont'd

10. (Amended) The method of claim 8, wherein said at least one predetermined property is such that at least one of the cobalt salicide regions has a predetermined conductivity.

12. (Amended) The method of claim 8, wherein the removal during step (e) of the cobalt layer from those MOS transistor structures where cobalt salicide exclusion regions are to be formed, and step (b), are performed in a manner significantly limiting cobalt salicide crawl during step (g) over and under at least one of the portions of the MOS structures where cobalt salicide regions are to be formed.

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Add the following new claim:

13. (New) A method for forming metal salicide regions and metal salicide exclusion regions during the manufacturing of an integrated circuit (IC), the method comprising the steps of:

providing an IC structure including a plurality of MOS transistor structures, the plurality of MOS transistor structures having exposed silicon surfaces;

A7

then, depositing a metal layer having a predetermined thickness over the IC structure;

then, forming a photoresist masking layer on those MOS transistor structures where metal salicide regions are to be formed;

then, removing the metal layer from those MOS transistor structures where metal salicide exclusion regions are to be formed;

then, stripping of the photoresist masking layer from those MOS transistor structures where metal salicide regions are to be formed; and